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# PETsys SiPM Readout System

The PETsys SiPM readout system is designed for reading a large number of SiPM photo-sensor pixels in applications where a high data rate and excellent time resolution is required. It is based on the TOFPET2 ASIC [1]. This is a low power ASIC with 64 channels optimized for reading SiPMs for Time Of Flight PET applications. The ASIC is the interface between the analog signals from the photo-sensors and the digital readout. Every time one of the 64 channels in the ASIC exceeds the thresholds, an event record is created giving the channel number, the time and the charge of the event. The rest of the readout chain only handles digital data. The default version of the ASIC is version 2.c; this version only reads positive signals. Version 2.d allows reading either positive or negative signals. For positive signals is it behaves very similar to ASIC2.c

The readout system has four main components: the Front-End Module, the Front-End type D module, the Clock&Trigger module and DAQ board. Together these boards allow assembling a complete and scalable data acquisition system reading tens of thousands of independent SiPM pixels.

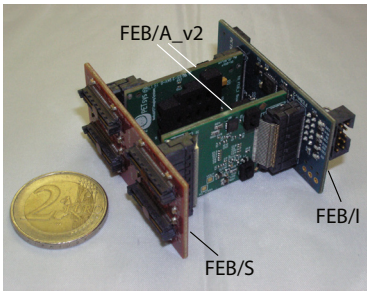


**Figure 1. FEM128**
The Front-End Module FEM128 has two ASICs and reads 128 SiPM channels. It measures 25.4x53.1x54.0 mm.

## The PETsys Front-End module.

The PETsys Front-End Module is the front-end readout module for reading SiPM arrays, or micro-channel plate photo-detectors. It is the interface between the analog signals of the photo-sensor and the digital readout chain.

The Front-End Module version FEM128 (Fig. 1) has 128 channels. It is optimized for systems requiring a high channel data rate. The Front-End Module is made-up from three different boards : FEB/A_V2, FEB/S and FEB/I. This allows for easy customization for different SiPM types and scanner geometries. A Front-End Module version FEM256 allows for a more compact detector geometry and is discussed later in this flyer.

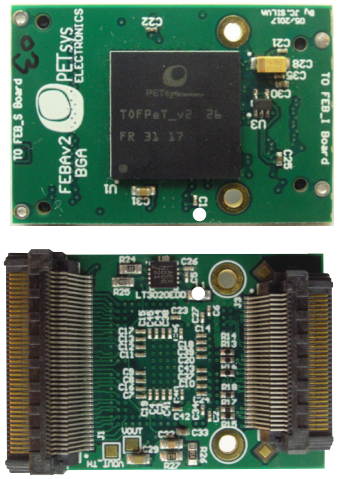

**Fig. 2: FEB/A_V2**
Top and bottom view. The connector to the right connects to the FEB/S, the connector to the left connects to theFEB/I . The board, including connectors, measures 39x25 mm.

The FEM128 has two FEB/A_V2 boards (Fig. 2). Each FEB/A board has one PETsys TOFPET2 ASIC with 64 channels. These boards are mounted perpendicular to the SiPM arrays, and this geometry makes it easier to control and stabilize the temperature of the SiPM array. The board also has a temperature sensor near to the ASIC.

The FEB/S board is a purely passive board adapting the SiPM array to the input connector on FEB/A_v2 board .This board will be different for different SiPM array models. The version of the FEB/S board shown on figure 1 has two pairs of connectors that directly take the Hamamatsu S13361-3050AS-08 8x8 MPPC array, or the KETEK 8x8 array PA3325-WB-0808. Each FEB/S measures 53.1 x 25.4 mm and is four-side buttable such as to allow forming a continuously sensitive area with almost no dead space. The FEB/S also has two temperature sensors, each located in the middle between the pair of connectors taking one SiPM array.

**Fig. 3: SAMTEC HQCD cable.**
A flat coax cable assembly connects the Front-End Module to the PETsys FEB/D board.

The FEB/I allows the FEB/D to communicate with both ASICs and the temperature sensor in the FEM128. It is equipped with a MAX 10 Altera FPGA and adapts the electrical communication protocol from LVCMOS in FEB/D to LVDS in the ASIC and reads the analog temperature sensors. Up to eight FEM128 can be connected to one FEB/D-1024 board using a SAMTEC HQDC-030-xx.00-TTL-SBL-1N flat cable (Fig3). It is also possible to plug the front-end modules directly into the FEB/D.

The power dissipation of the ASIC is 8.2 mW/channel for the recommended settings. The LVDS buffers and LDO voltage regulators of the FEM add 6mW/channel and bring the total power consumption of the FEM at 14.2 mW/channel. The data output of the ASIC uses 4 LVDS data lines at up to 800 Mbps per data line. The events are encoded in 80 bits. The maximum event rate between the FEM128 and the FEB/D is about 500 kcps per channel.

[1] Experimental characterisation of the TOPET2 ASIC, R. Bugalho et al., JINST_079P_0918

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## The PETsys Front-End type D module.

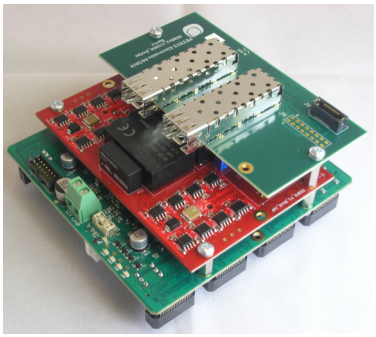

Figure 4: FEB/D module.
Top view of the FEB/D_1024 module showing the bias voltage mezzanine (red) and the DAQ mezzanine on top of it..

The Front End type D module (FEB/D-1024) is shown on figures 4 and 5. It provides power for the ASICs, adjustable bias voltages for the SiPMs, configuration, clock & synchronization signals, and data readout for up to 8 FEM128. It is composed of a FEB/D motherboard with a Kintex-7 FPGA_XC7K160T, a communication mezzanine, and a bias voltage mezzanine.

Each FEB/D mother board measures 104.5x104.5 $mm^2$.

Eight front-end modules FEM128 can be connected to one FEB/D-1024 board, using either direct board-to-board connectors or using flexible coaxial flat Samtec cables (Fig. 3). The 12V power DC-DC converters and regulators on the FEB/D motherboard provide the low voltages (1.9 V and 3.6 V) for the FEM128.

The upper mezzanine on figure 4 is the communication mezzanine. It has a SFP+ port for data output to the DAQ and for receiving the configuration signals. A second SFP+ port allows the FEB/D to be daisy chained. The SFP+ ports operate at 6.6 Gbit/s allowing a maximum event output rate of 100 Mcps.

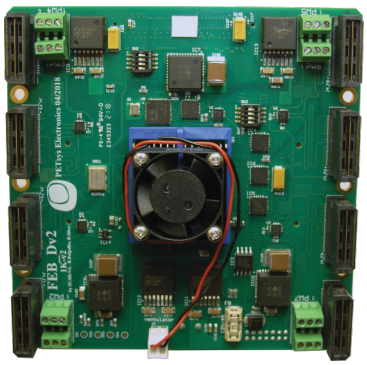


Figure 5.
Bbottom side of the FEB/D-1024 mother board showing the 8 connectors receiving the cables from the FEM128 modules.

Synchronous readout of multiple FEB/D modules is enabled by a connection to the Clock&trigger module through a ERNI SMC connector carrying LVDS signals at 400 Mbit/s. This interface also provides for a trigger system allowing to discard events that are not part of a coincidence, in the FEB/D before transmission.

A Gbit Ethernet communication mezzanine is also available for use with small systems. When using the Gbit Ethernet communication mezzanine the maximum data output rate to the computer is 15 M events/s.

The middle mezzanine on figure 4 supplies bias voltages to the SiPMs. The de fault mezzanine provides 16 positive bias voltages in the range 0-72 V, with a maximum current of 2.5mA per bias line. We can provide a version providing a maximum current of 8.75 mA per line. We also can provide a different bias voltage mezzanine with 64 bias voltage lines, same voltage range, 8per FEM128.In this case the maximum current is 550mA per bias line. It is possible to connect an external power supply and in this way provide up to 50 mA per bias line.

A customized mezzanine version, supplying a larger current, can be developed on request.

## Main features of the FEB/D-1024 module:

- Reading up to 1’024 independent SiPM channels from 8 FEM128.
- Equipped with Kintex 7 FPGA.
- Comes with pre-installed firmware.
- Connects to up to eight Front-End Modules with 128 channels.
- Choice of two Data output DAQ mezzanines: SFP+ optical/copper, or Ethernet.
- Max output rate 6.6 Gbps, or 100 M events/s.
- Up to 32 FEB/D-1024 boards can be Daisy chained and connected to a single DAQ board input.
- Receives clock and synchronization signals from the Clock&Trigger module.
- Clock frequency 160-200 MHz.
- External supply voltage:  12 Vdc, maximum 4 A.
- On board DC-DC converters supply power to the ASICs in the FEM boards.
- SiPM bias voltages produced in a mezzanine. The default mezzanine provides 16 lines, 5-100 V, positive, 3-9 mA per bias line.
- Can accept a veto signal  from the Clock&Trigger module..



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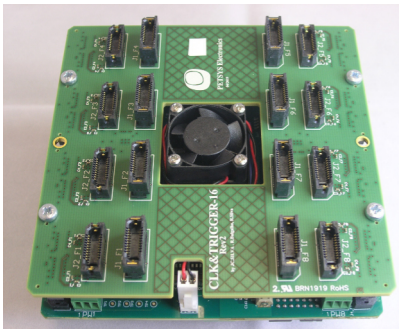


Figure 6: Clock&trigger module.
Bottom view showing the connectors for 16 Samtec ERCD cables providing clock an trigger signals to the FEB/D modules.

## The Clock&trigger module.

The Clock&trigger module (fig. 6) provides synchronization and time coincidence filtering for the FEB/D modules. All FED/D modules connect to the Clock&trigger module using a flat coax cable Samtec ERCD-010-80.00-TBR-TBR-1-N. The Clock&trigger module allows implementing a system wide coincidence filter, collecting coarse time information from all the FEB/D modules and transmitting only coincidence events.

The Clock&trigger module also generates the system reference clock and synchronization signal. For synchronization with external systems, it can accept an external clock and synchronization signal or it can provide a clock and synchronization signal to an external system. It can also accept a veto signal which causes all events across all FEM to be discard when it's active.

The Clock&trigger module uses the same mother board as the FEB/D board. It also has the same communication mezzanine and uses the same communication protocol, and connects to the DAQ board in the same way. The Clock&trigger board supports up to 16 FEB/D and 4 trigger regions per FEB/D. A Clock&Trigger board for larger systems can be developed on request.

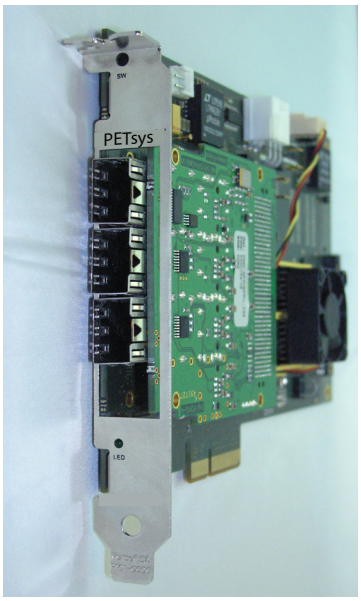


Figure 7: DAQ board.
The DAQ board plugs directly into the PCI express bus of the DAQ computer. The three SFP+ connectors on the front panel receive the 3 SFP+ copper links or optical links from the FEB/D chains.

## The PETsys DAQ Board

The PETsys DAQ board (Fig. 7), is equipped with a Kintex-7 FPGA. It collects data from the FEB/D boards, and transmits the data to the DAQ board in the DAQ computer using a x4 PC express port.

The standard version of the DAQ board has 3 SFP+ optical/copper connectors connecting to 3 chains the FEB/D boards transmitting data at 6.6 Gbps (Fig. 8).

The DAQ board receives and merges the data frames and transmits the assembled data frames to the computer. The maximum event rate to the DAQ computer is 200 Mcps. The DAQ board also sorts the events in the data frames by chronological order to facilitate processing by software.

Several FED/D boards can be daisy chained and send their output over the same optical link to the DAQ board. In this way the DAQ board, the Clock&Trigger module and the FEB/D modules together form a complete and scalable data acquisition system that can handle tens of thousands of SiPM channels.

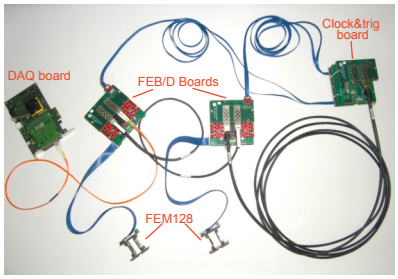


Figure 8.
The DAQ board is connected to the FEB/D modules and the clock&trig module using a SFP+ copper link or optical link.

## Main features of the DAQ board:

- Single PCI express board providing data acquisition with TOF ASICs.
- Equipped with Kintex7 FPGA.
- Compatible with FEM128, FEM256, FEB/D1024 FEB/D4096, and Clock&Trigger modules.
- Equipped with 3 SFP+ optical/copper connectors receiving three optical links for sending and receiving data to/from three FEB/D module chains.
- Distributes configuration files for the ASICs.
- Configures the Clock&Trigger module.
- Maximum total input event rate: 100 M events/s for each of the input links.
- Maximum data output rate to the DAQ computer: 200 M events/s.
- Reads temperature sensors in the Front-End Modules.
- Reads of TOF ASIC dark counters.
- Accepts an external veto signal and distributes it to the FEB/D boards via the Clock&Trigger module.



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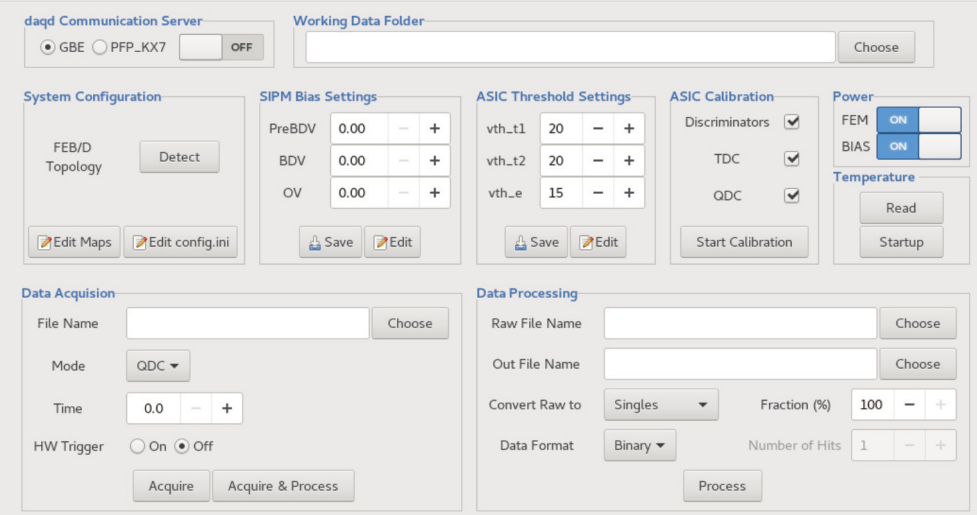
Fig. 9: Graphical user interface.
The data acquisition is controlled by an easy to use graphical user interface




## Firmware and software

The PETsys readout system is provided with firmware and software. The data acquisition software runs under Linux and comes with an easy to use graphical user interface, see figure 9. The software is written in Python and C++, and is also provided as source code, allowing the advanced user to customize it.

The firmware implements a software centric approach, allowing direct and online access to PETsys TOFPET 2 ASIC configuration, bias voltage configuration, temperature sensor readout and also to raw TOFPET 2 ASIC data.

In order to reduce the data rate and discard events without interest, the firmware in the FEB/D modules supports coincidence event selection. The coincidence selection is based on coarse time stamps (1 clock period, 5 ns). The complete readout is divided in a configurable number of trigger regions, and events without a coincidence partner in a different trigger region are discard in the FEB/D boards before transmission. The smallest trigger region consists of two FEM128 connected to the same FEB/D1024. Besides the optional rejection of events that are not part of a coincidence, no other manipulation is performed on the raw event data from the TOFPET 2 ASIC.

The coincidence filter searches for coincidences between events above a configurable energy threshold, belonging to allowed trigger region pairs. The time difference between coincidence events is configurable to 0, 1, 2 or 3 clock periods.When coincidences are found, the coincidence filter will forward any events within a window (3... 16 clock cycles) of the primary trigger events. The duration of the windows and the matching of the trigger regions is configurable. The coincidence filter allows collecting of data for two types of random coincidence correction methods:

• Wide coincidence window: The coincidence window can beset to a value larger than2 clock cycles, allowing the collection of more random events; this is broadly equivalent to the delayed window method.

• Periodic single trigger: In addition to coincidences, the trigger can select all events in a window of 10, 20, 50 or100 clock periods every1025 clock periods. The1025 clock periodicity ensures that the data collected is de-correlated from the systems' 1024 clock frame period.

## Synchronization with other systems.

It is often necessary to synchronize the clock on the PETsys readout with other clocks in the system. If the ratio of the clocks frequencies of the two sub systems is an integer, both can share a common clock and synchronization signal. The FEB/D board or the Clock&trigger module can accept an external signal and generate a event record with a time least count of 1.24 ns. Alternatively, one can use any ASIC input channel to generate time event records with a timing least count of 30 ps. Finally the Clock&trigger module can send out LVDS timing signals synchronized to the ASIC clock at a configurable frequency.



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## Examples of readout solutions.

The readout was developed with the application in Time of flight PET in mind, but can also be used in may other applications where one needs to read a large number of SiPM pixels. The Front-End Modules, the Front End type D module, the DAQ board and the Clock&Trigger module together allow building data acquisition systems adapted to the needs of most applications. Below we present 4 typical applications in PET.

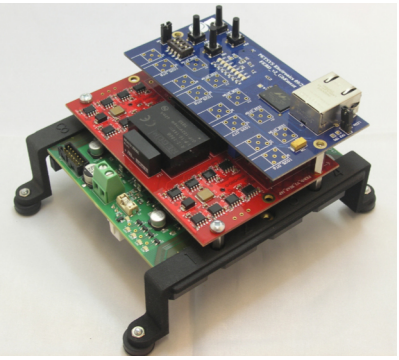


**Figure 10. FEB/D for small systems.**

Figure showing a FEB/D1024 module with Ethernet mezzanine. The FEB/D1024 module collects data from up-to eight FEM128, and sends the data to a computer using an Ethernet link at 1Gbit/s.

## Readout solution for small systems.

If the application requires1'024 channels or less, and if the total data rate to the computer is below 15 M events/s after coincidence event selection, the readout will need one FEB/D-1024 equipped with an Ethernet communication mezzanine (Fig. 10), and maximum eight FEM-128.

For the purpose of coincidence event selection, the Front-End Modules connected to one FEB/D can be grouped in maximum four trigger regions. A trigger region consists of either one or two FEM128.

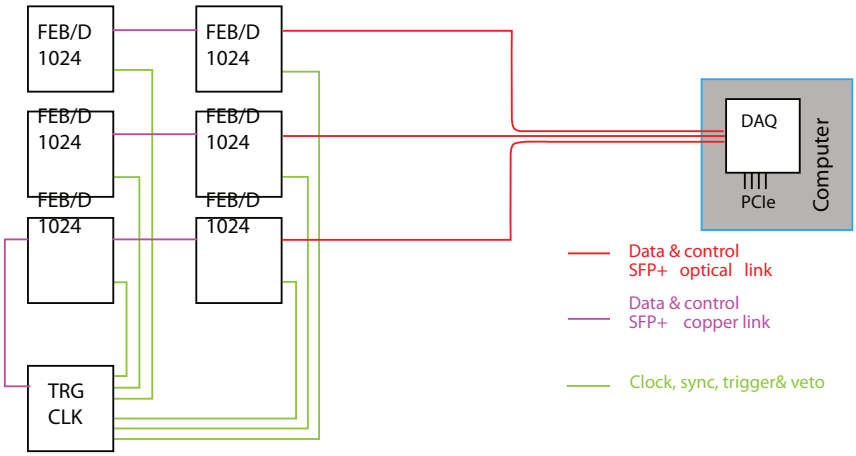
## Readout solution for several 1'000 channels.

If the application requires reading more than 1'024 channels, or requires a larger event rate to the computer, the system needs a Clock&Trigger module and a DAQ board, see figures 6 and 7. Figure 11 shows system interconnect topology for a system with 6'144channels. It can be extended to more channels by daisy chaining more FEB/D-1024 boards. One chain of FEB/D boards can have up to 32 boards. Each ASIC has 4 LVDS data output links, and the maximum data output rate from the ASIC to the FEB/D-1024 is 500 kcps per ASIC channel.

In most cases the data rate from the DAQ board to the computer (200 M events/s) will be limiting the event rate per channel. The useful event rate will depend on the efficiency of the coincidence filter. The efficiency of the coincidence filter depends on the geometry of the PET scanner considered; it typically reduces the data rate to the computer by a factor 10. For example, in a PET system with 6'144 channels, the maximum single event data rate the system can handle is of the order of 500 kcps foreach channel.

**Figure 11. System with 6'144 channels.**

System interconnect topology for a readout with 6 FEB/D1024 boards. Each FEB/D1024 is connected to eight FEM128. In this example the communication between the master FEB/D module and the DAQ computer uses optical fibers, and the communication between the FEB/D modules in the FEB/D daisy chain uses SFP+ copper links.

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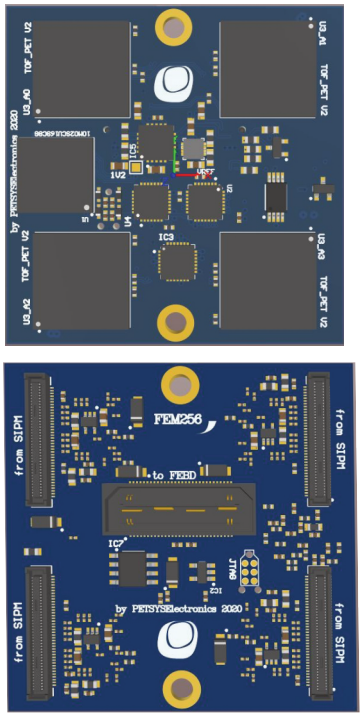


Figure 12. FEM/256 board.
The figure above shows the two sides of the FEM256 board.

## Readout solution for several 10’000 channels.

A version of the readout solution with a front-end module reading 256 channels (FEM256) and a FEB/D4096 reading 4096 channels is available. It is optimized for a lower per channel cost in applications such as Whole Body PET were data rates are lower. In the FEM256 module only 2 data output lines per ASIC are used and the maximum event rate from the ASIC to the FEB/D is 300 kcps per channel.

Figure 12 shows the FEM256 board. It has 4 PETsys TOFPET ASICs and connects to the FEB/D boards using the same Samtec cable shown on figure 3. This FEM256 board connects to the FEB/S with the SiPM arrays with a flat flex cable as shown in Figure 13. The aluminum cooling plate in this figure is only shown to illustrate the cooling concept to be used in this case. The user can adapt the cooling to his particular scanner geometry. The FEB/D_4096 connects to 16 FEM256. This readout solution uses the same Clock&Trigger module and the same DAQ board as the readout with FEM128 and FEB/D1024 modules.

Figure 14 shows the system interconnect topology of a system reading 32’768 channels. The system has 8 FEB/D4096, 128 FEM256, one DAQ board and one Clock&trigger module. The useful event rate per channel will be limited by the data transfer rate to the computer. In this example the maximum event rate per channel will be 60 kcps if the coincidence trigger reduces the data rate by a factor 10. Using the same DAQ board and the same Clock&trigger module the system can straightforwardly be extended to reading 65’636 channels.

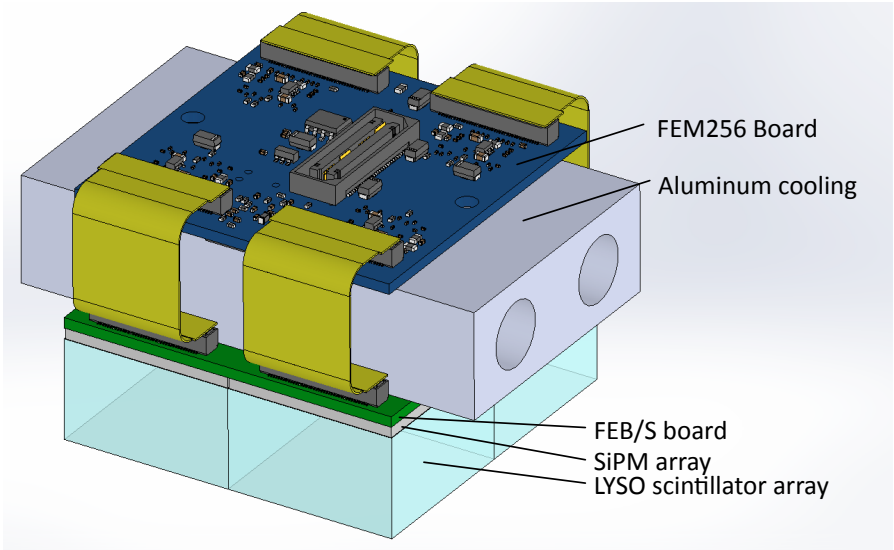


Figure 13. FEM/256 detector module.
The figure to the left illustrates how to build a detector module based on the FEM256 board. The cooling solution must be adapted to the particular scanner geometry. .

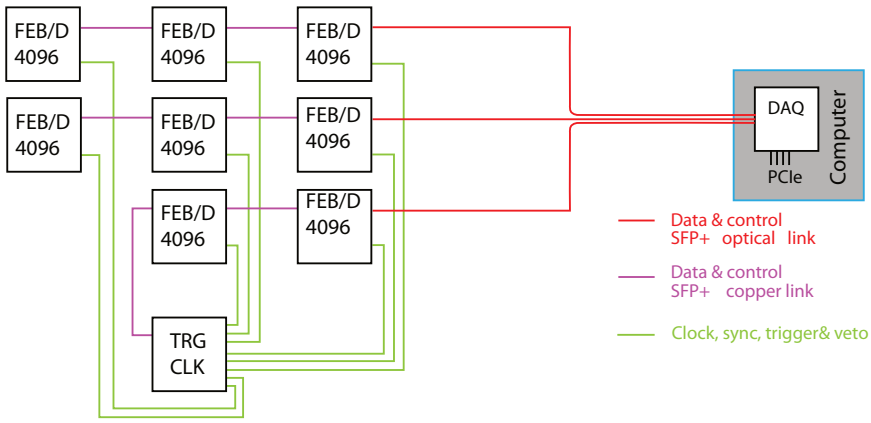


Figure 14. Readout for a system with 32’768 channels.
System interconnect topology for a system reading 32’768 channels. The system has 128 FEM256 boards connected to 8 FEB/D_4096.

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## Readout solution for reading 100’000 channels.

A total body PET scanner requires reading several 100’000 SiPM pixels. If every SiPM pixel has its own readout channel this will require several DAQ boards to allow for a sufficient data rate to the computer. Figure 15 shows the interconnect topology for a system reading 491’520 electronic channels. This example has 120 FEB/D4096 modules, one Clock&trigger module and 4 DAQ boards. The system uses the same FEM126, FEB/D4096 and DAQ boards as the system with a few 10’000 channels discussed before. Only the Clock&trigger module will be different from the standard Clock&trigger module.

There are ways to reduce the number of electronic readout channels in this application by using one of several multiplexing schemes. Contact sales to learn more about the possible options.

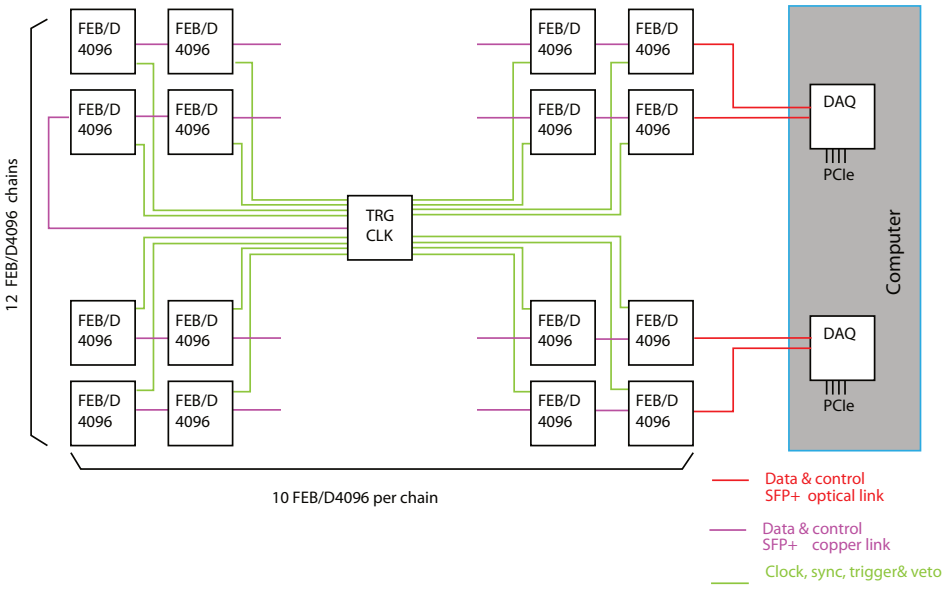


**Figure 15. Readout for a system with 491’520 channels.**

The systems has 4 DAQ boards and 12 chains with 10 FEB/D4096 modules each. Three chains of FEB/D4096 are connected to one DAQ board using one optical link. To simplify the figure only two DAQ boards, and two optical links per DAQ board, are shown.

For more information visit our web site www.petsyselectronics.com
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